

# GA-F2A78M-HD2

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APU\_VDDIO\_SUS=DDR15V  
APU\_VTT\_SUS=DDRVTT  
APU\_VDDP\_RUN=APU\_VDDR\_RUN=APU\_VDDP  
  
+1.1V\_RUN=FCH\_VDD\_11\_RUN=VCC\_SB  
  
+3.3V\_RUN=VCC3  
+3.3V\_ALW=3VDUAL

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Title

**COVER SHEET**

Size

Custom

Document Number

**GA-F2A78M-HD2**

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Thursday, January 23, 2014

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**Model Name:GA-F2A78-HD2**

## Component value change history

**Version: 3.0**

**Tip/Top : 9MF278HD2-00**

**P-Code: U13127-0**

[illegible]

### Circuit or PCB layout change for next version

[illegible]

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Title
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## BOM & PCB HISTORY

Size	
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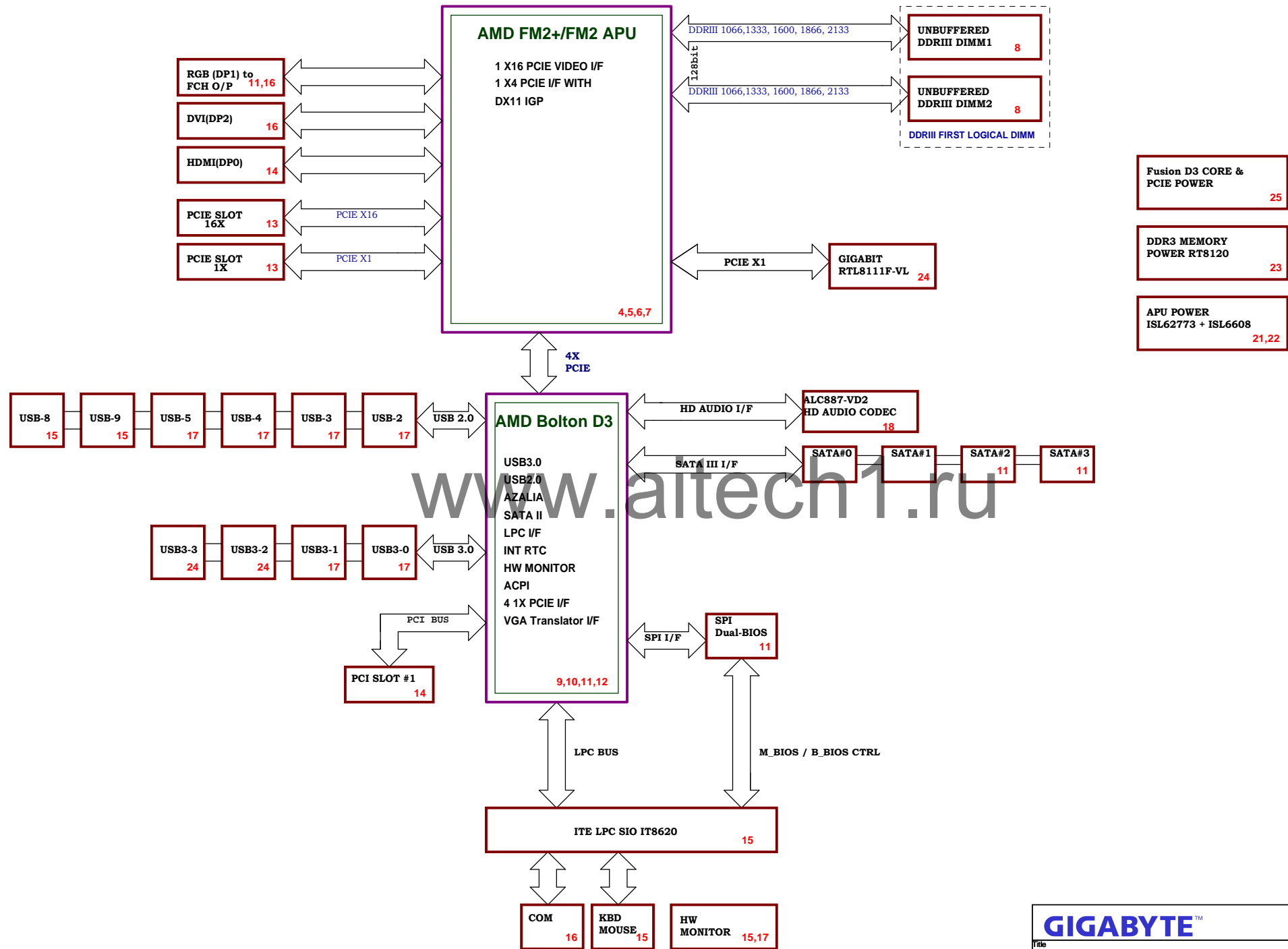
Document Number
-----------------

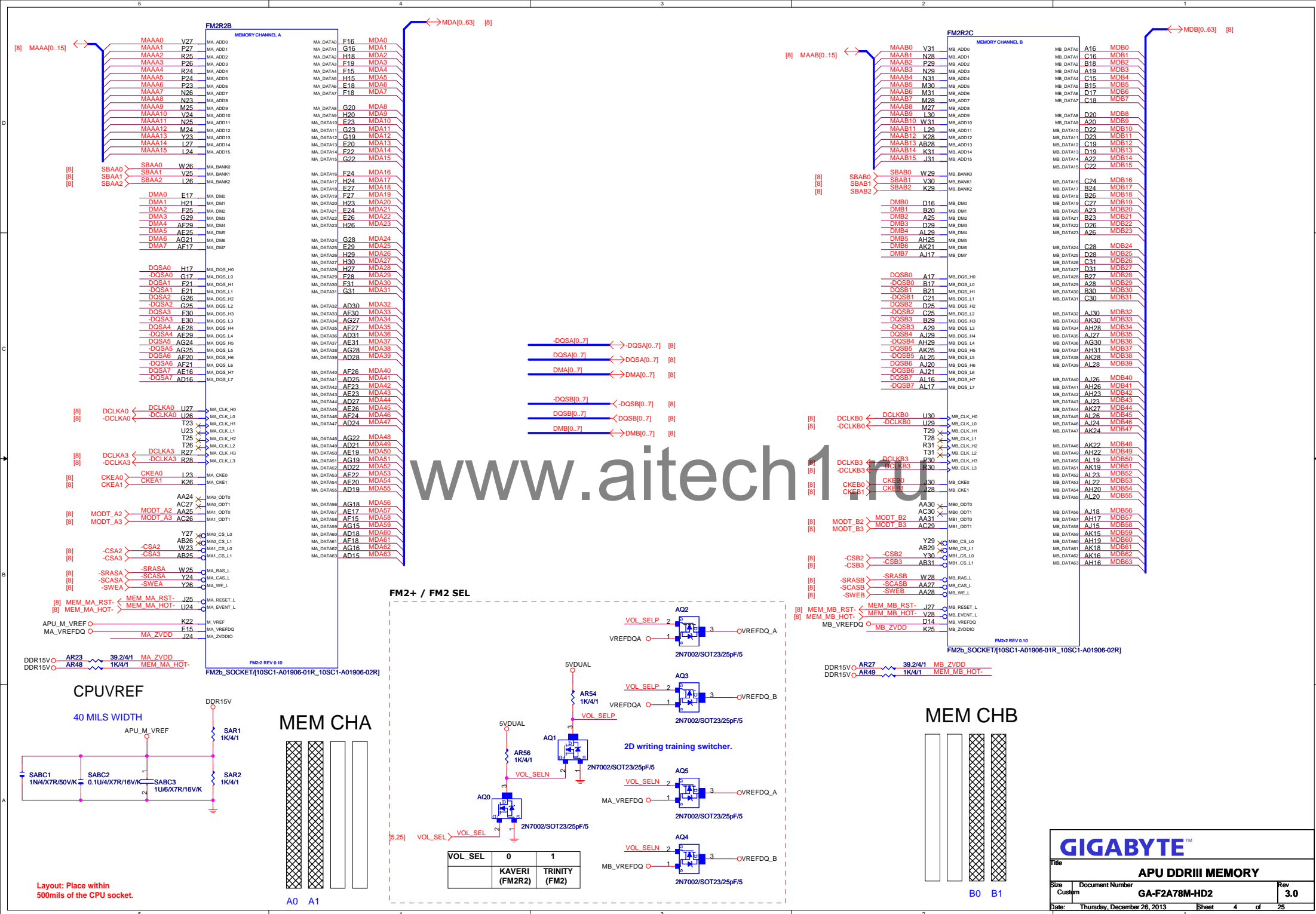
GA-F2A78M-HD2

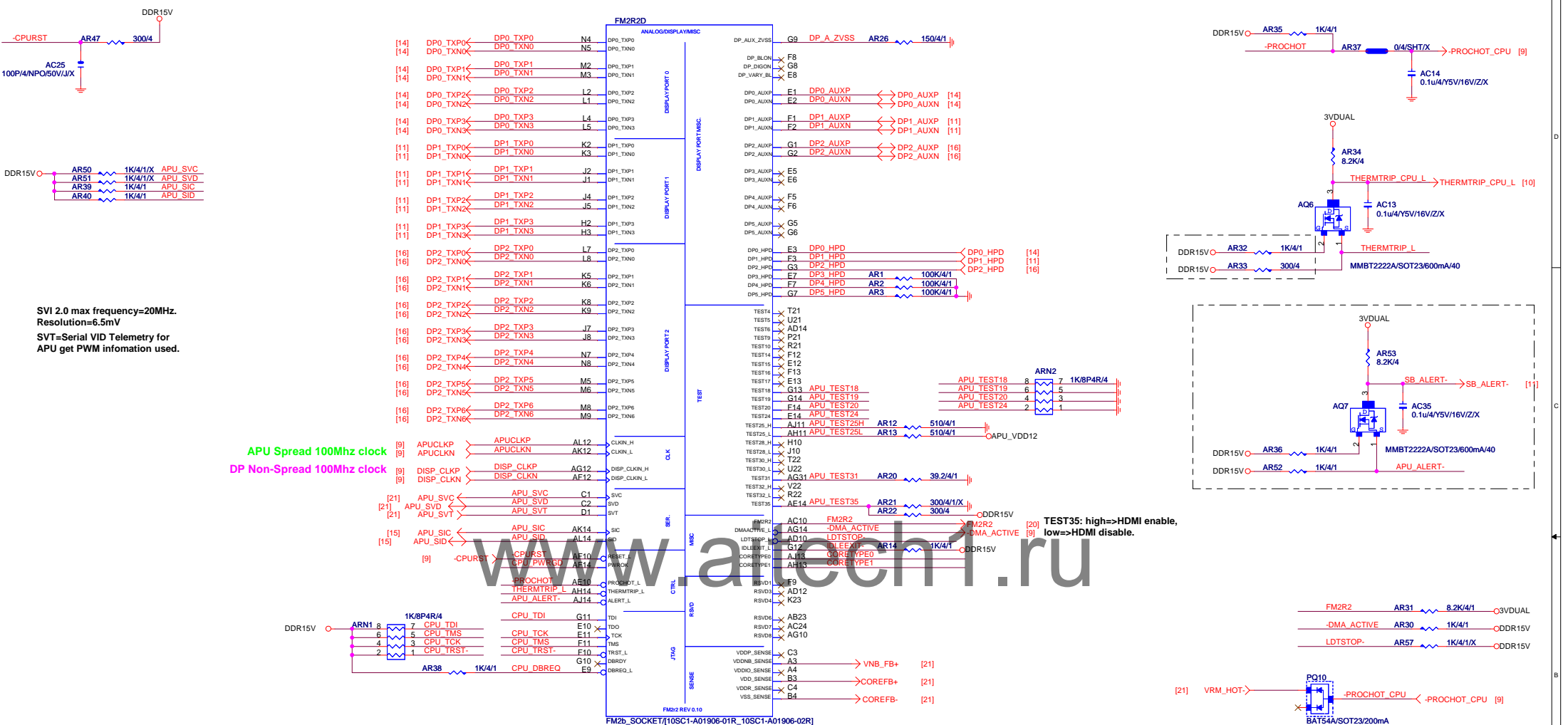
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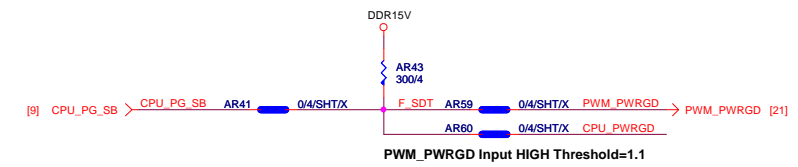




SVI 2.0 max frequency=20MHz.  
Resolution=6.5mV  
SVT=Serial VID Telemetry for  
APU get PWM information used.

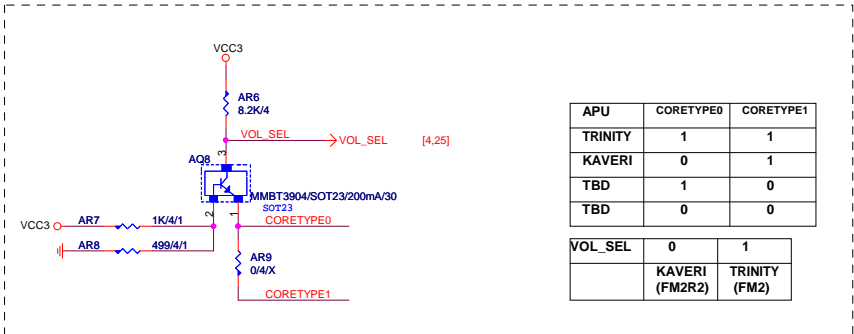
APU Spread 100Mhz clock  
DP Non-Spread 100Mhz clock

TEST35: high=>HDMI enable,  
low=>HDMI disable.



PWM\_PWRGD Input HIGH Threshold=1.1

### FM2+ / FM2 SEL



APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)

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APU CONTROL

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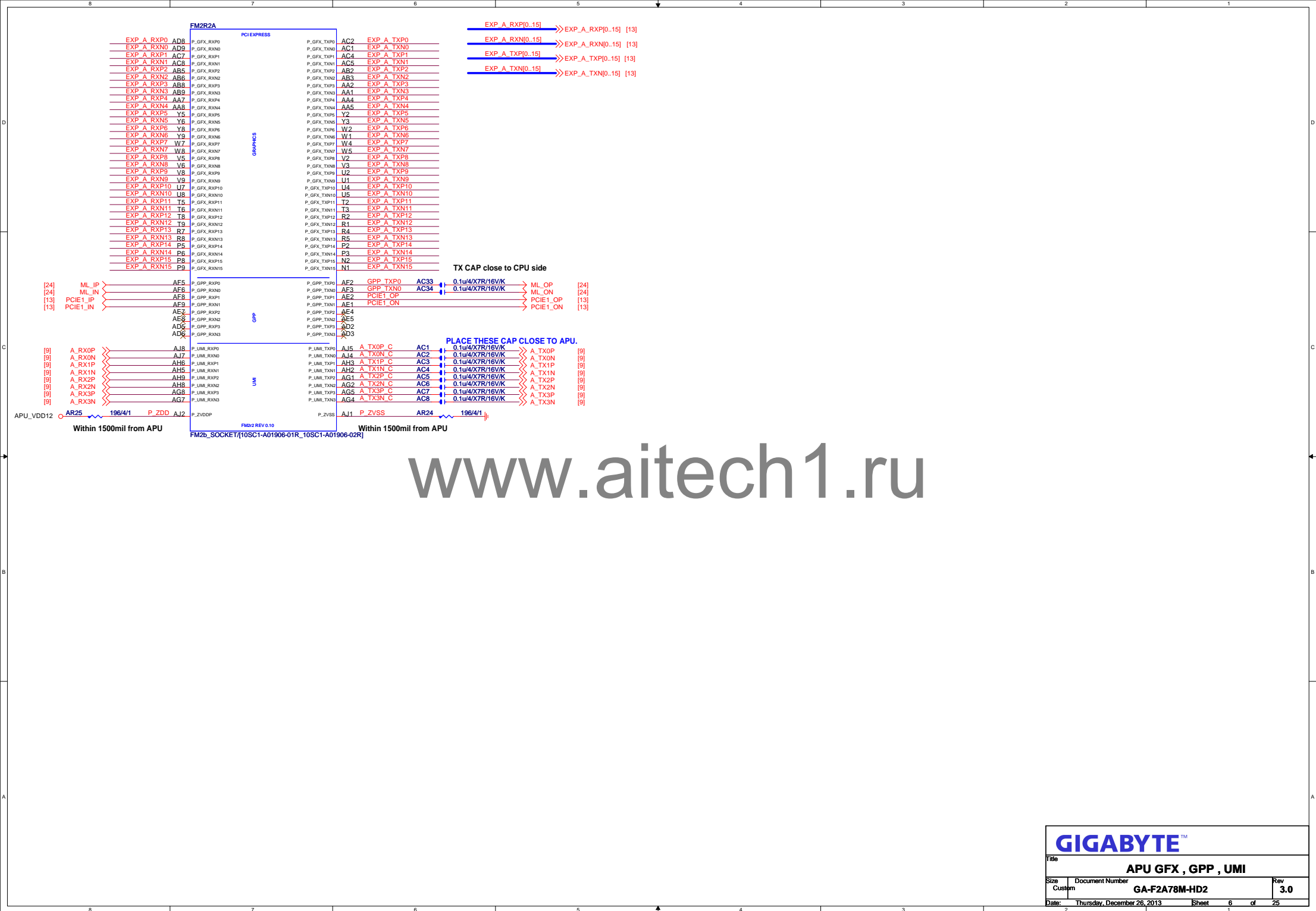
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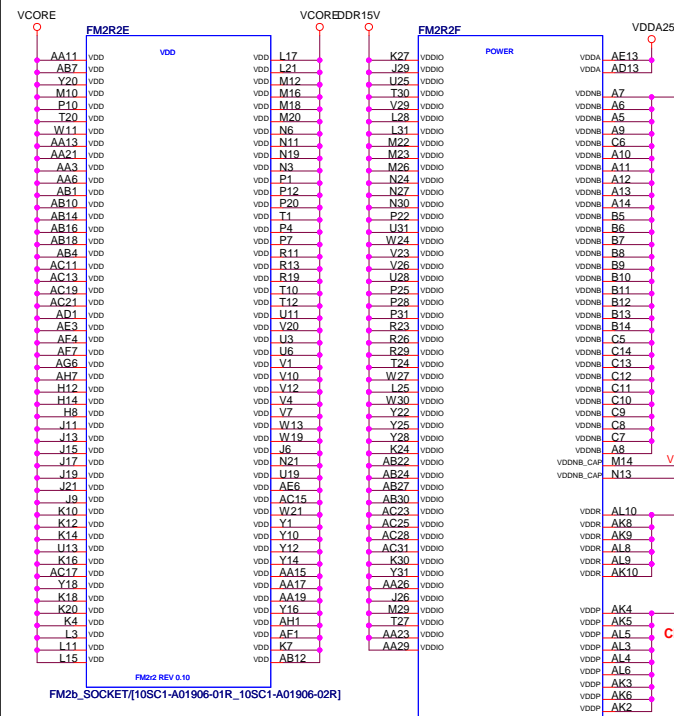
of

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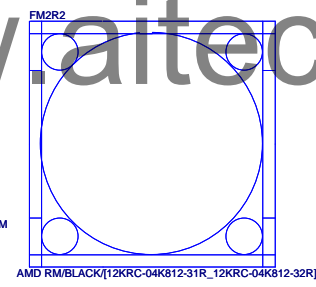
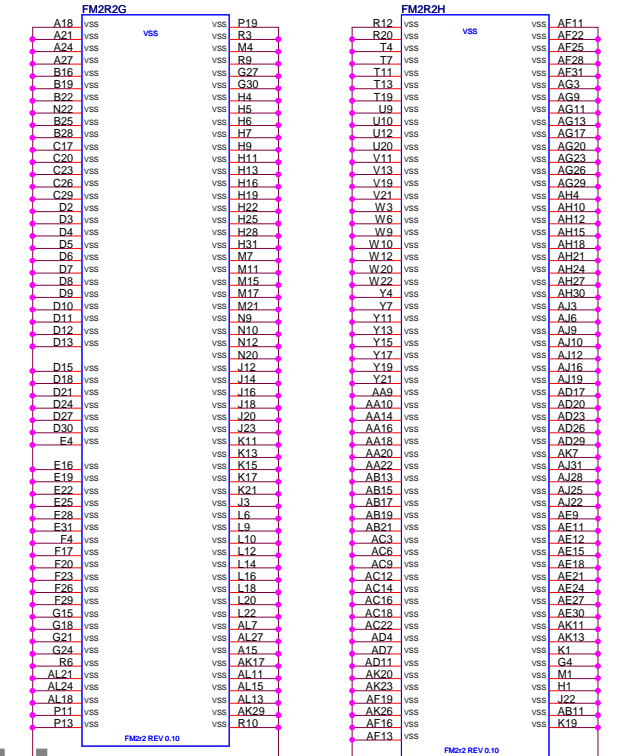
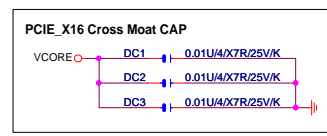
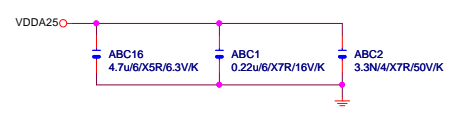


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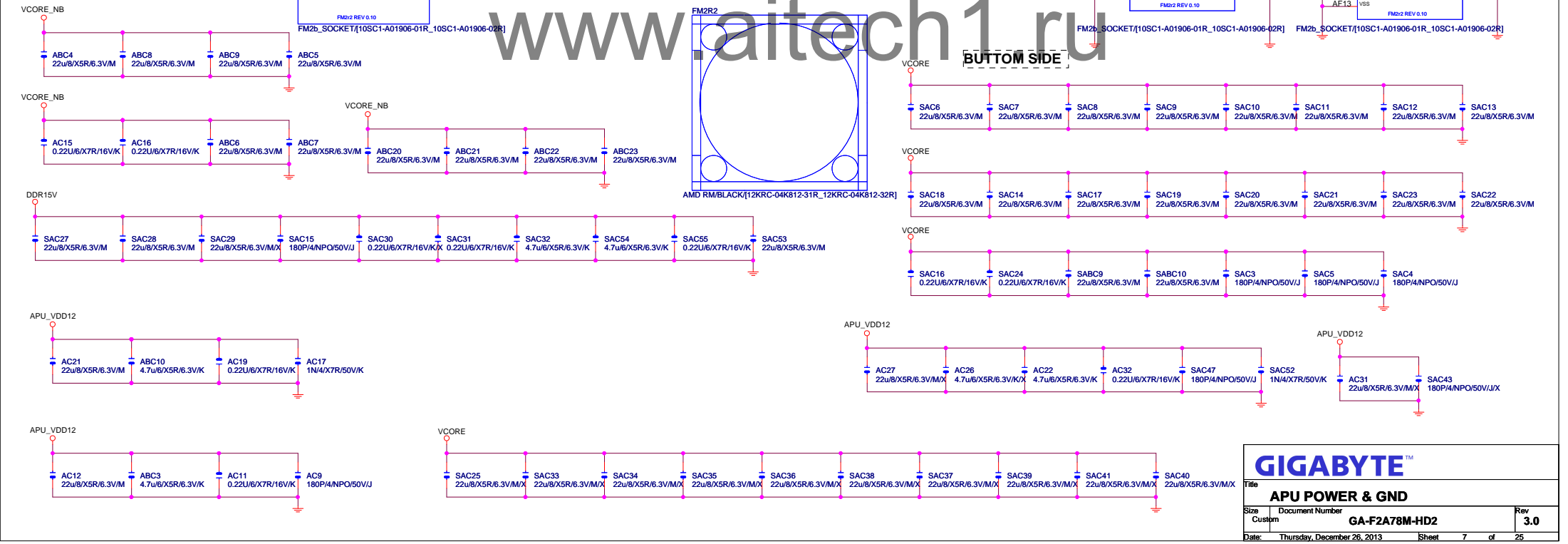
DDR15V=1.25V/1.35V/1.5V(DDR3)



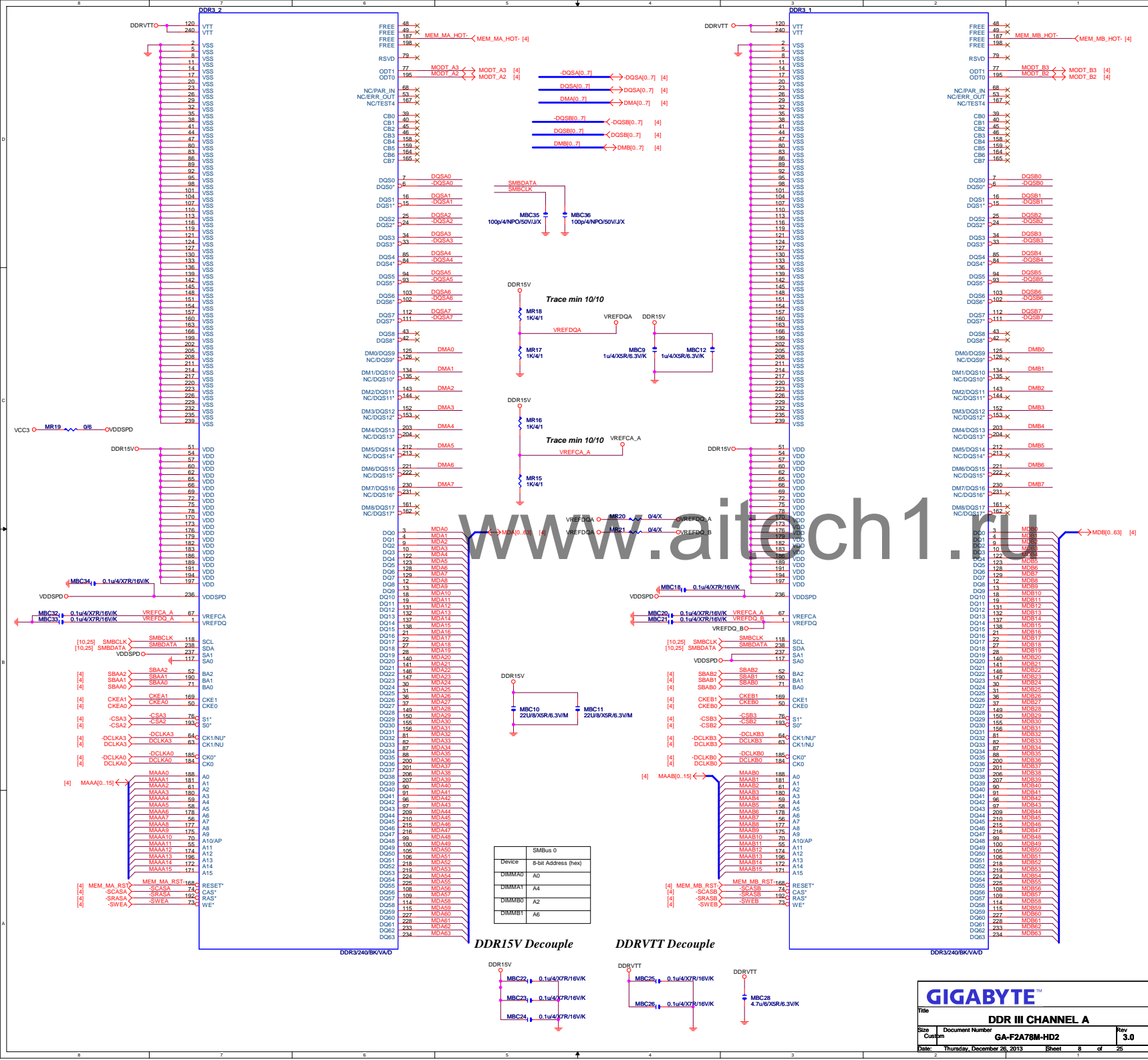
GND:232 pin,  
VCORE:99 pin,  
VCORE\_NB: 30 pin,  
DDR15V:49 pin,  
VDDP:9 pin, VDDR:9  
pin, VDDA25:2 pin,  
VDDNB\_CAP:2  
pin,Total:430 pin.



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Title APU POWER & GND			
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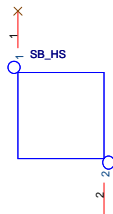




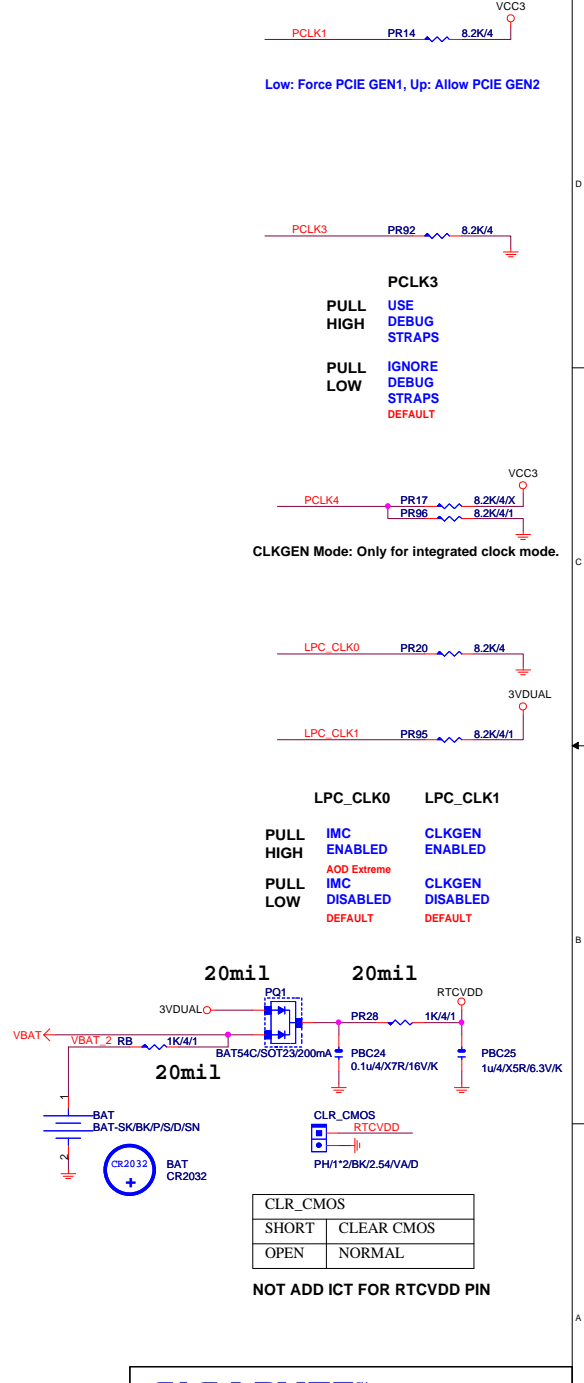
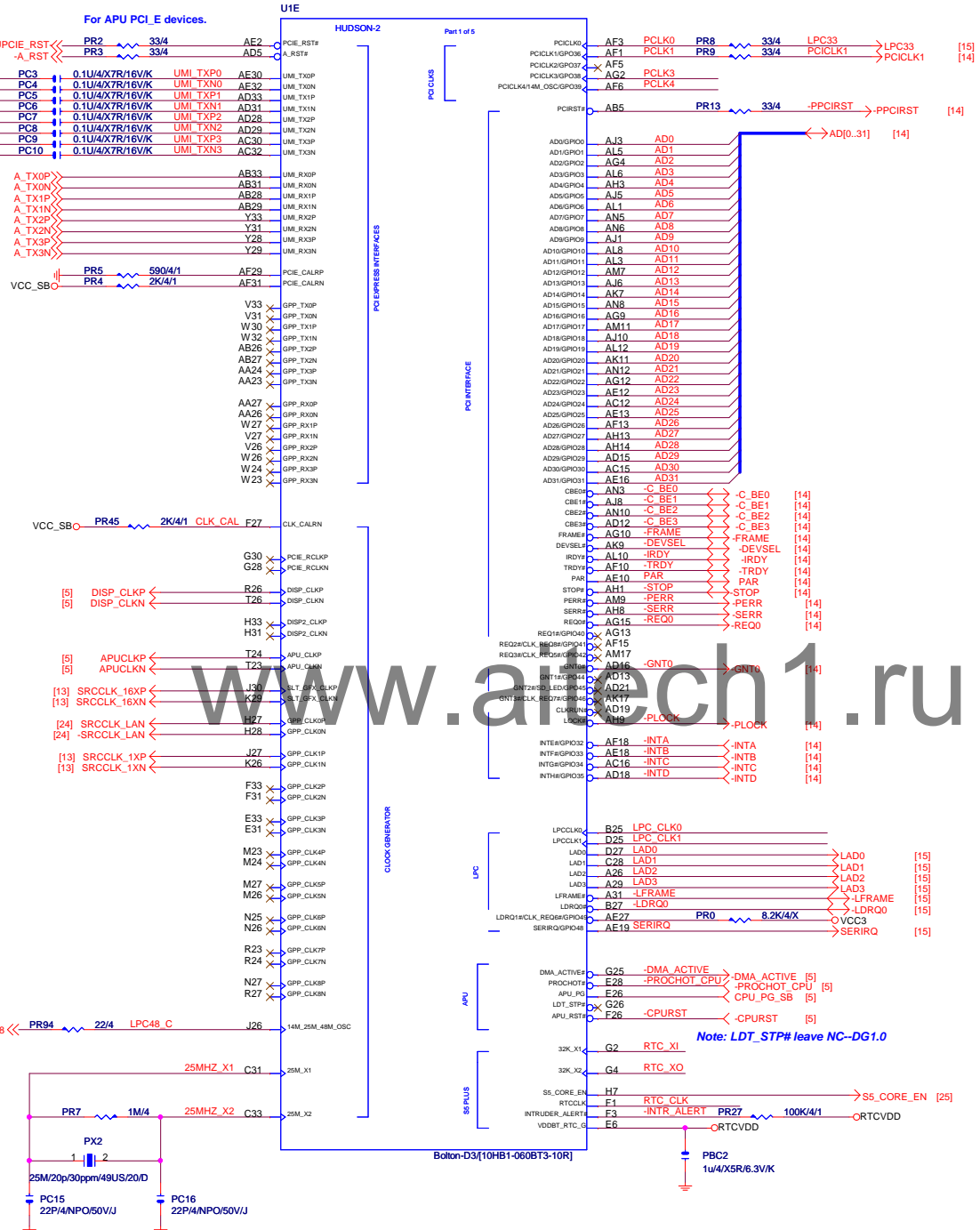
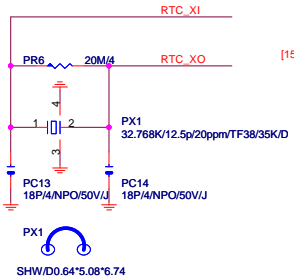


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

### S.B HEATSINK



SB\_HS[12SP2-SA0301-01R\_12SP2-SA0301-02R\_12SP2-SA0301-03R]



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**BOLTON D3 PCIE/PCI/CPU/LPC**

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Low: Force PCIE GEN1, Up: Allow PCIE GEN2

**PULL HIGH** USE DEBUG STRAPS  
**PULL LOW** IGNORE DEBUG STRAPS DEFAULT

CLKGEN Mode: Only for integrated clock mode.

**LPC\_CLK0** IMC ENABLED  
**LPC\_CLK1** IMC DISABLED  
**CLKGEN** ENABLED  
**CLKGEN** DISABLED

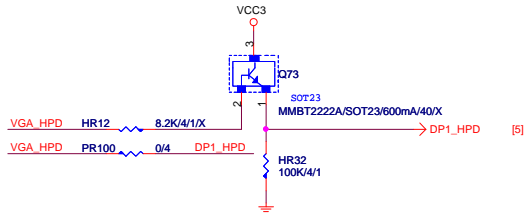
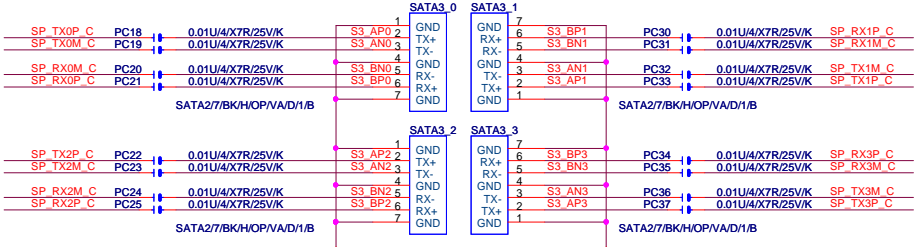
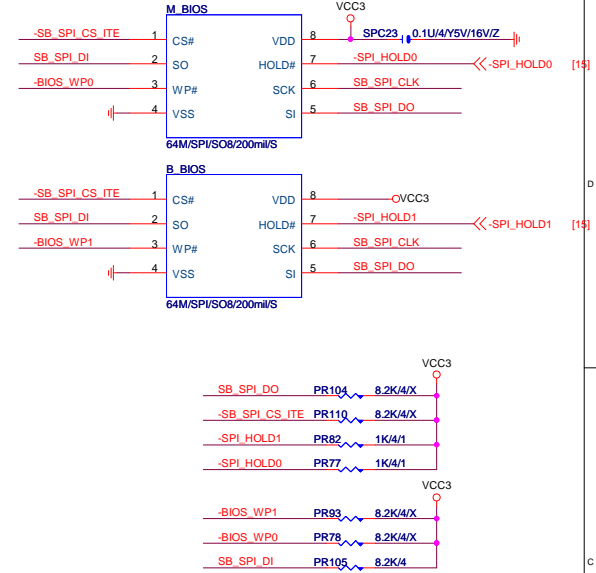
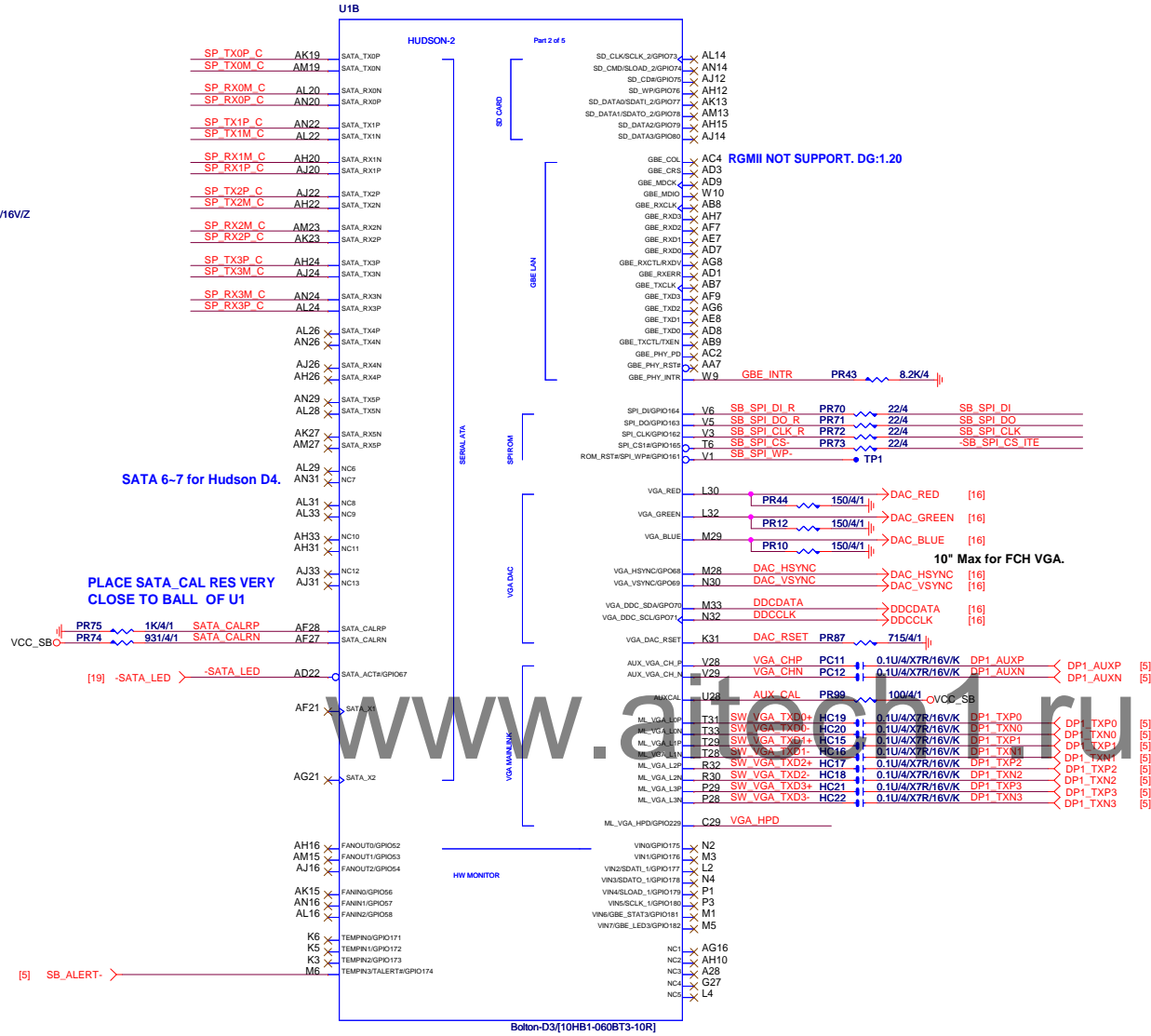
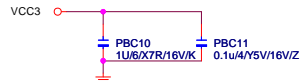
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

Note: LDT\_STP# leave NC-DG1.0

Pull down for S5+ Mode





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Title

**BOLTON D3 SATA/HWM/SPI**

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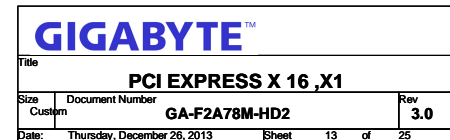
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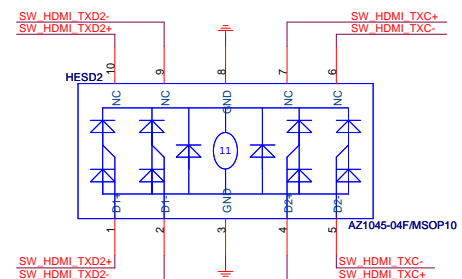
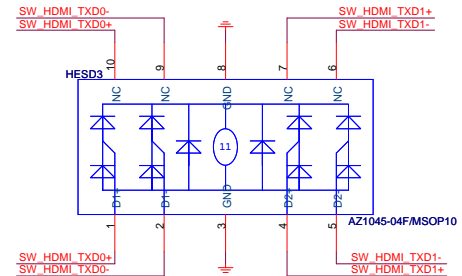
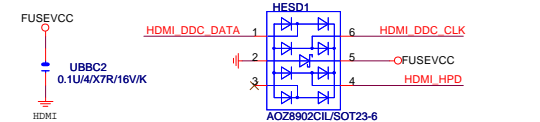
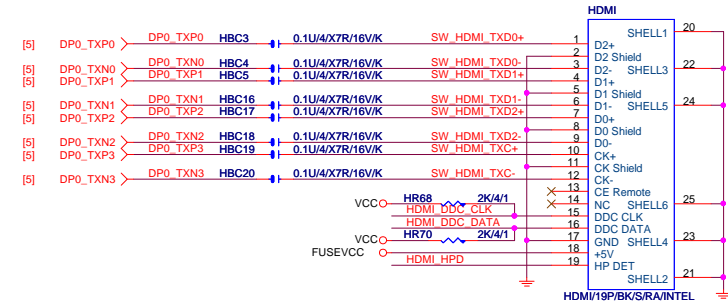
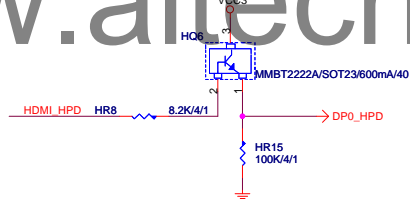
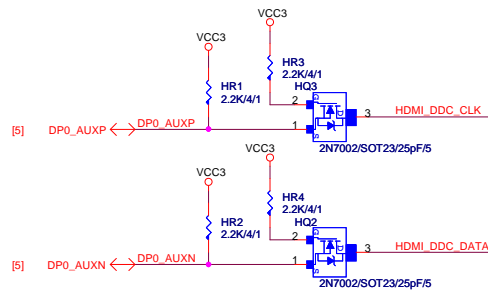
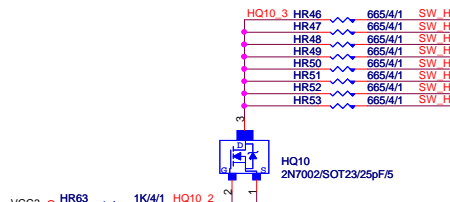
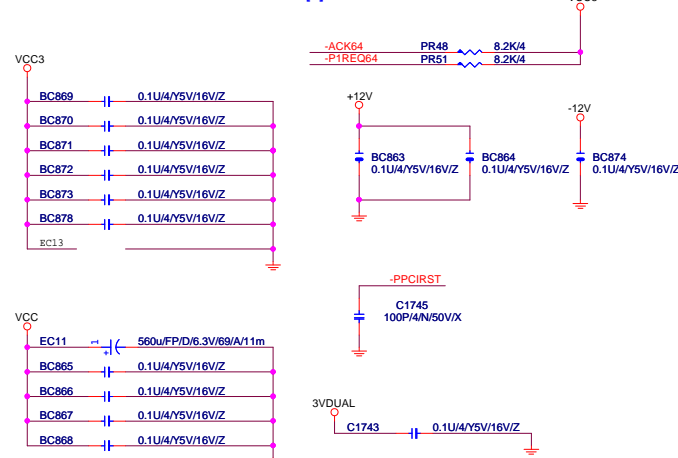
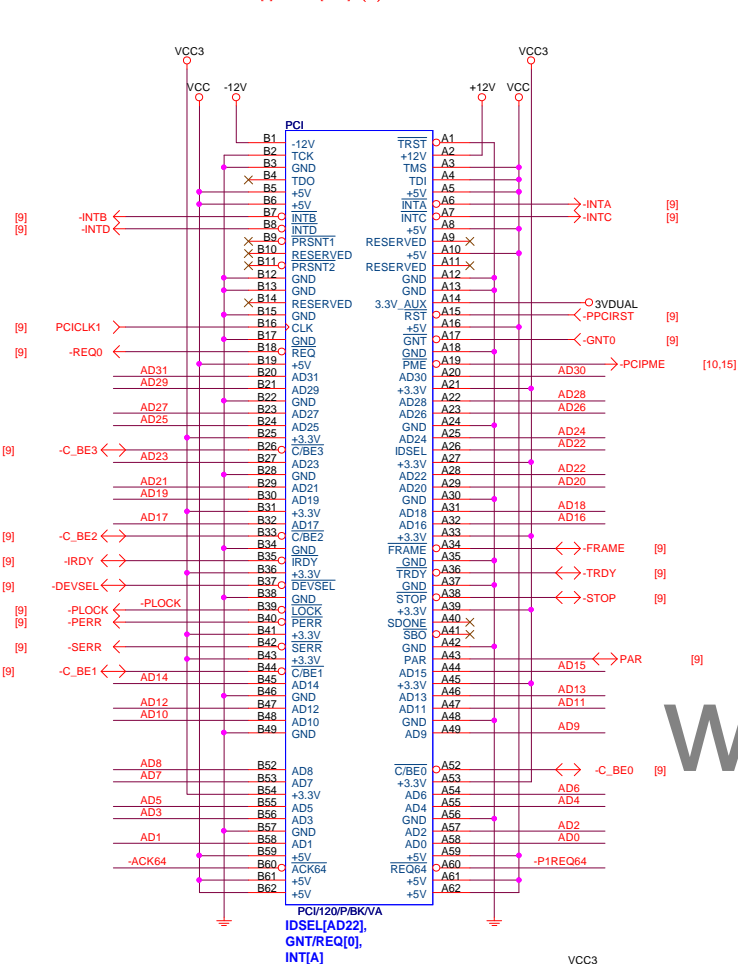
25





# PCI SLOT 1,2

[9] AD[0..31] <-> AD[0..31]



**HDMI,PCI SLOT**

Size Custom

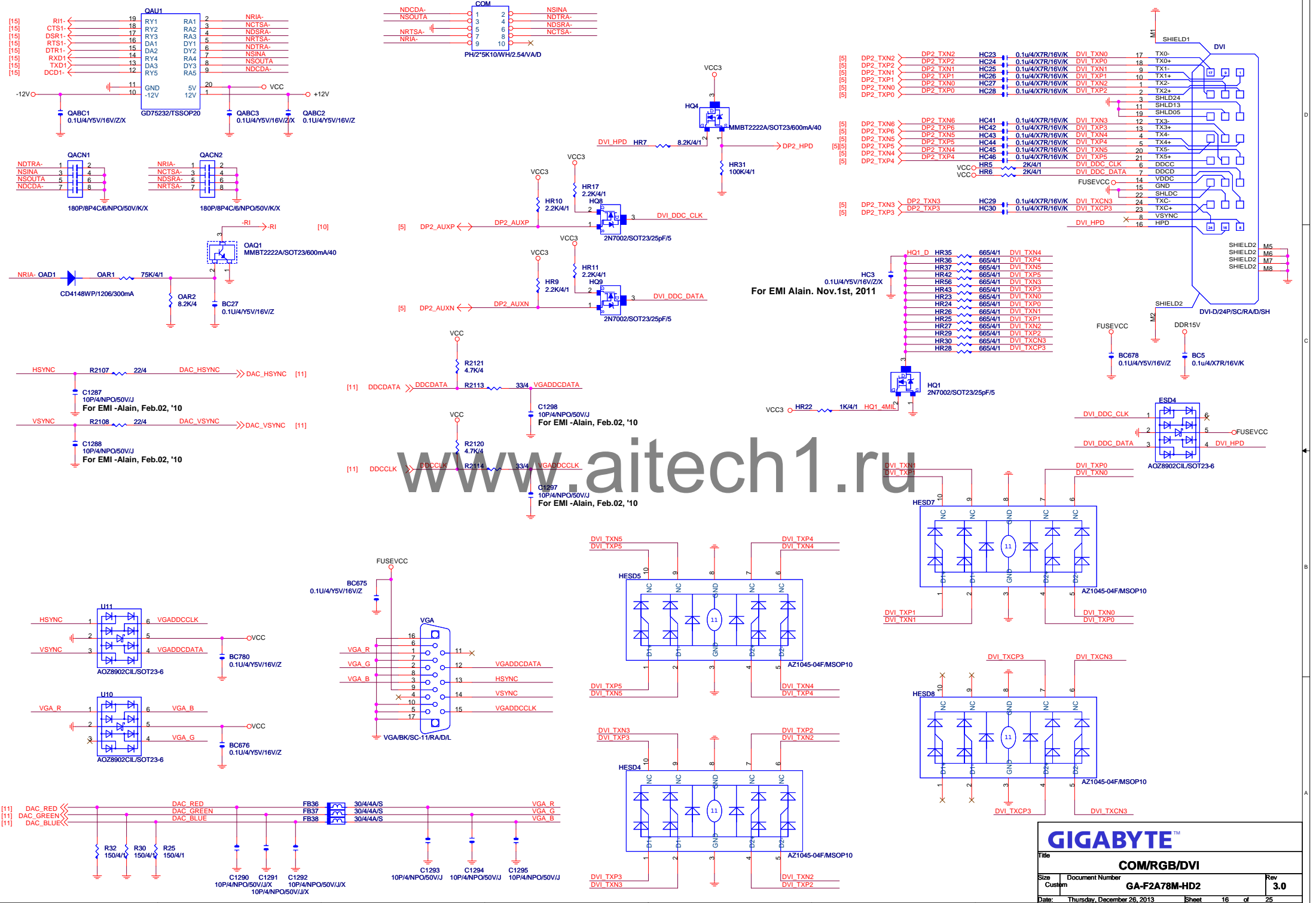
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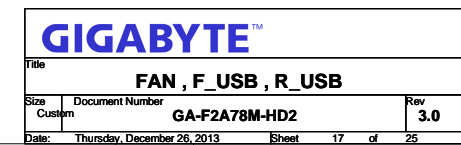
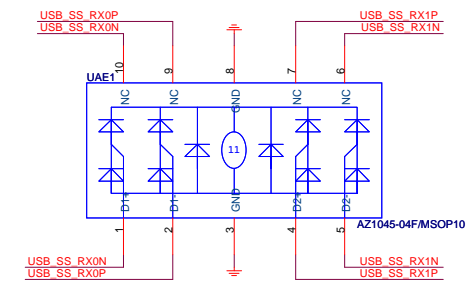
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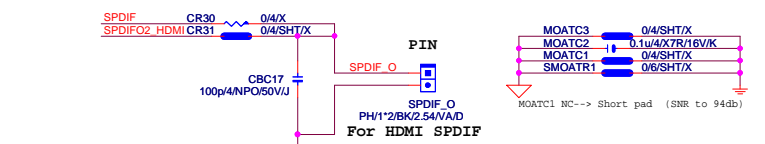




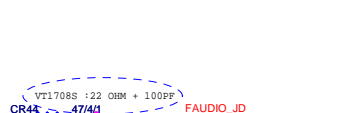
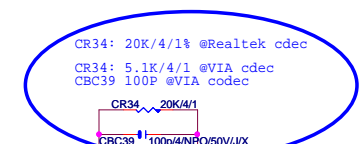
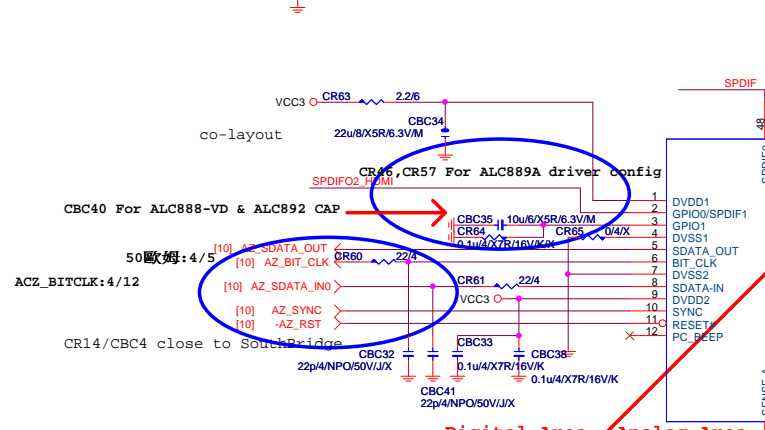
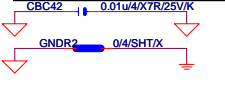




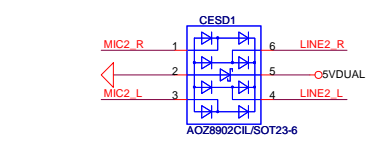
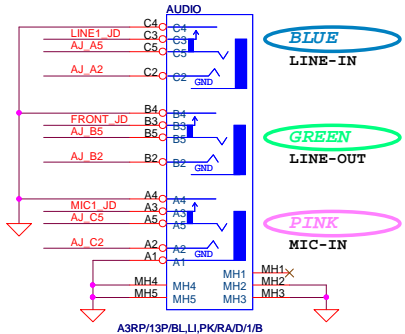
SPDIF\_OUT



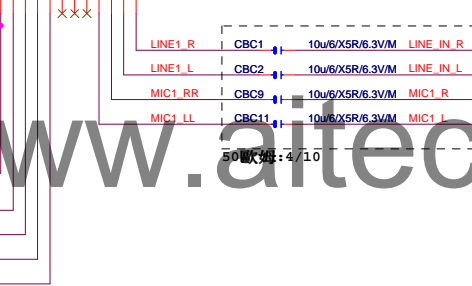
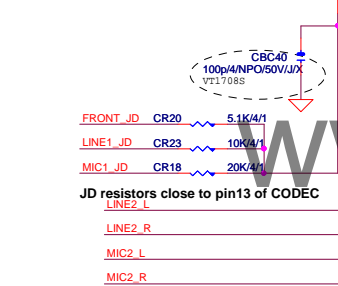
CODEC POWER/EMI PAD



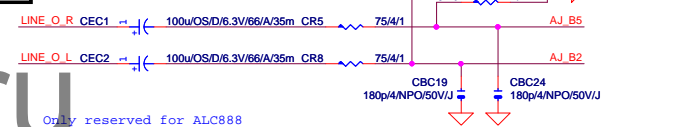
ADD CD2 For ESD PROTECT DIODE



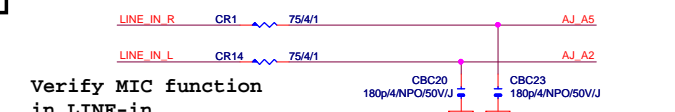
Digital Area Analog Area



LINE-OUT

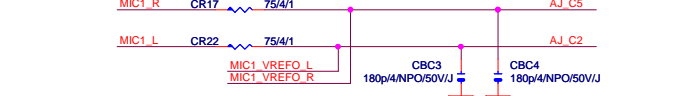


LINE-IN



Verify MIC function in LINE-in

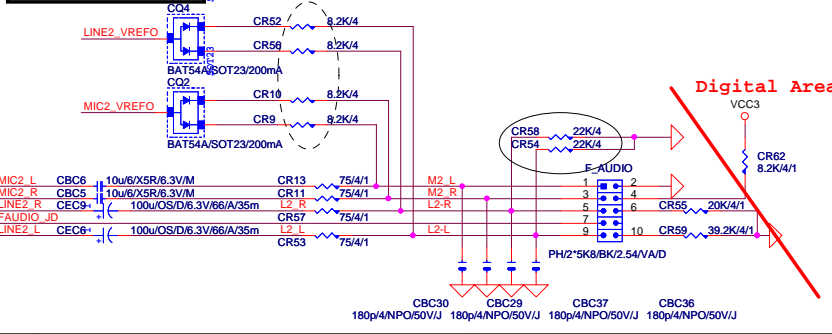
MIC-IN



AZALIA CODEC ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

AZALIA FRONT PANEL



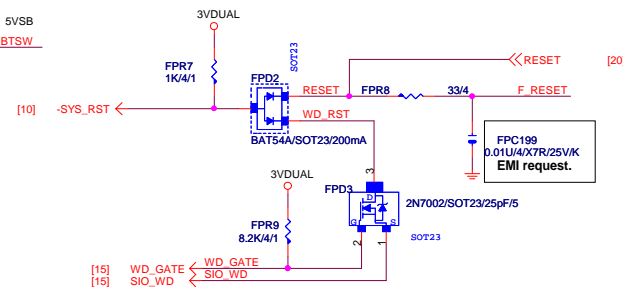
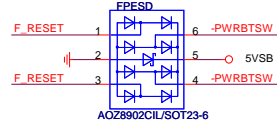
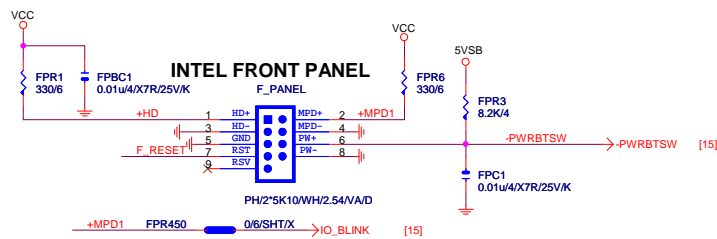
**GIGABYTE**

HD AUDIO ALC887-VD2

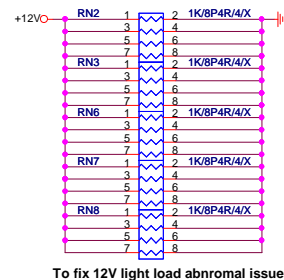
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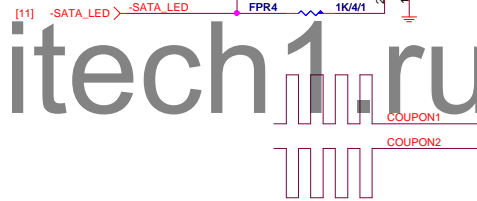
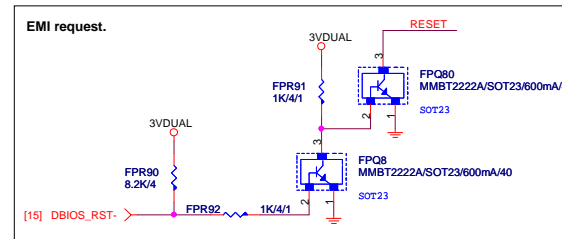
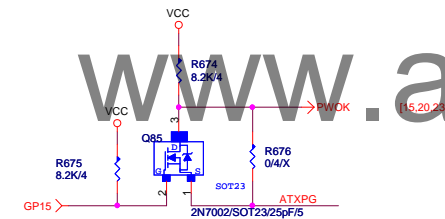


#### 【技術通報R&D技術通報153】

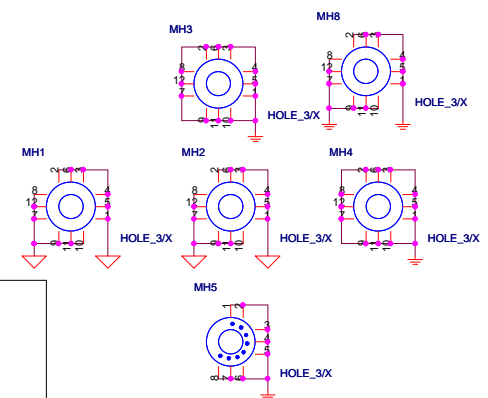
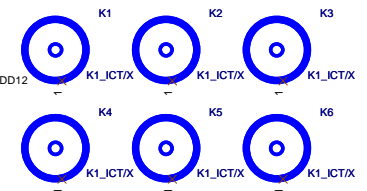
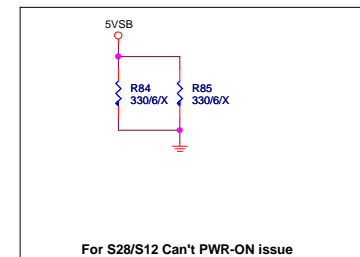
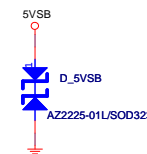
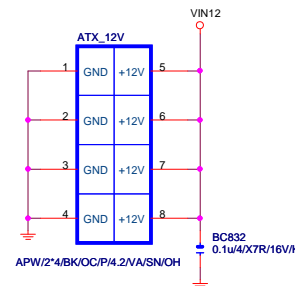
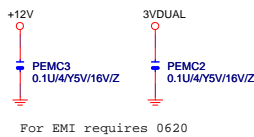
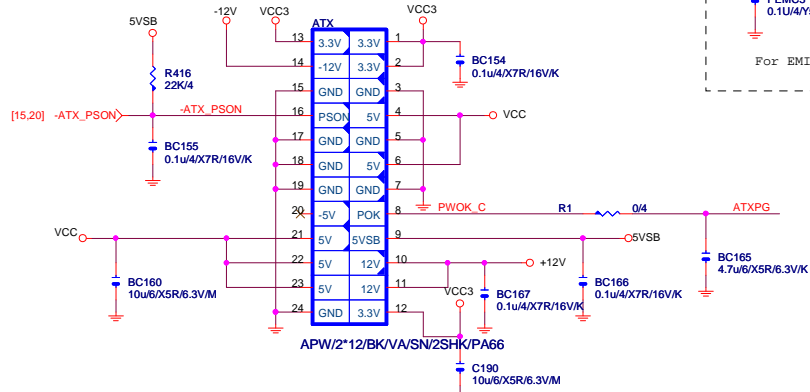


#### 【技術通報R&D技術通報154】

##### PWOK PATCH



#### ATX POWER CONNECTOR

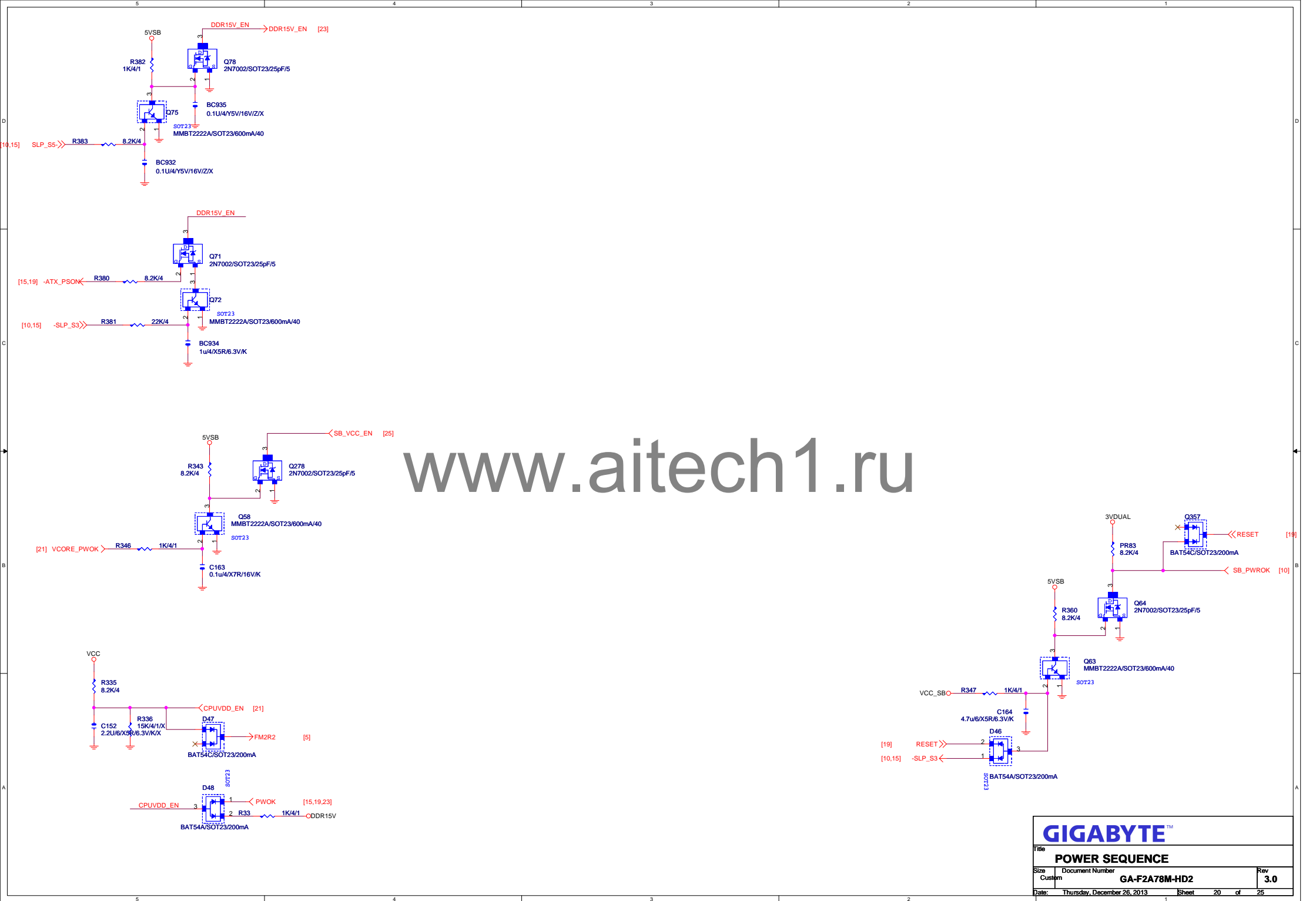


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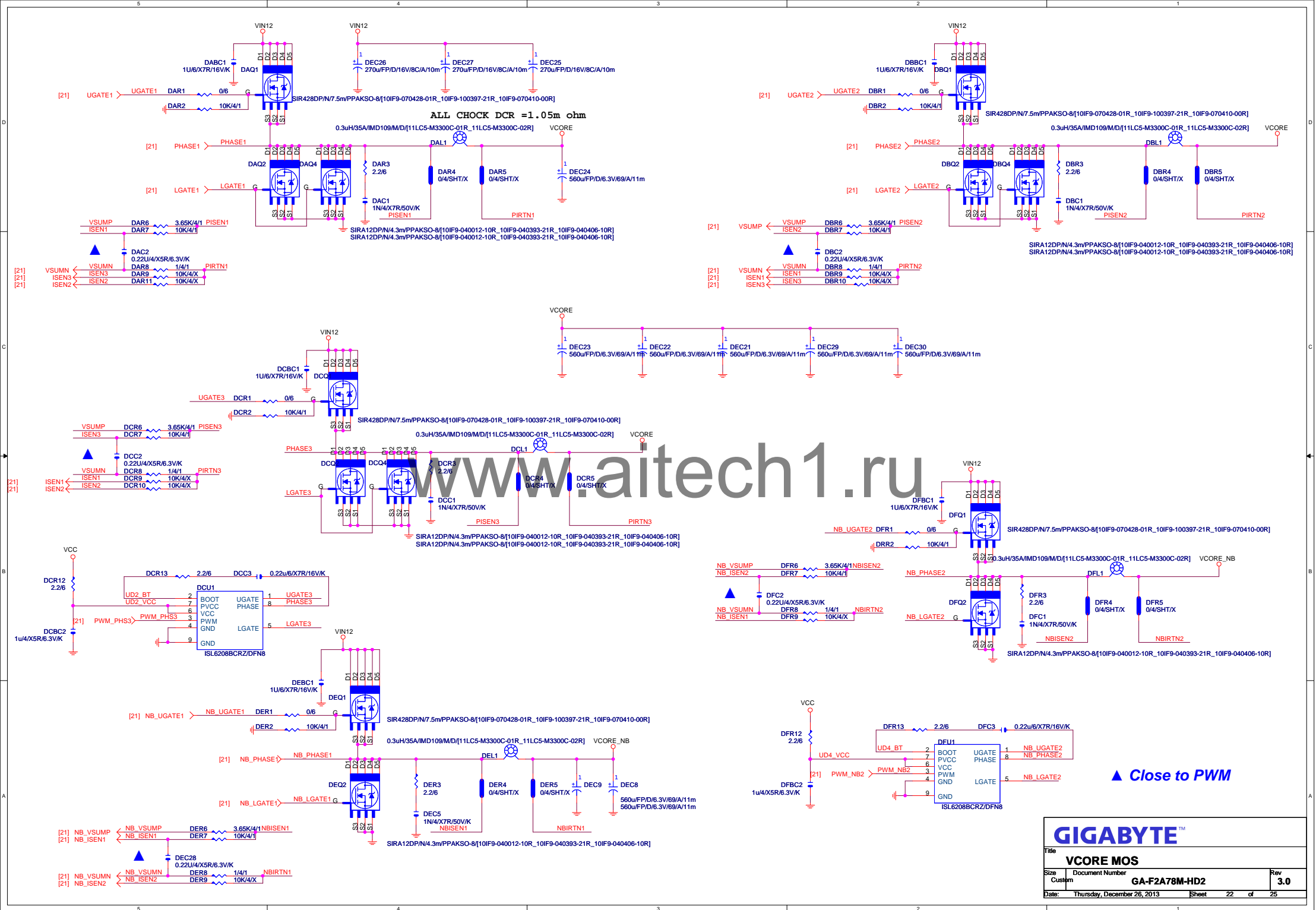
Title **ATX, FRONT PANEL**

Size Custom Document Number **GA-F2A78M-HD2** Rev **3.0**

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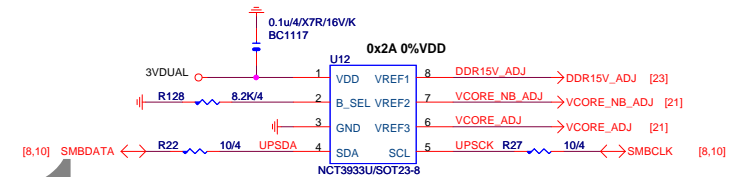
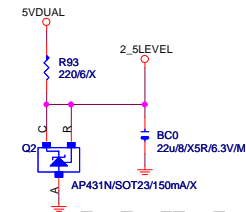
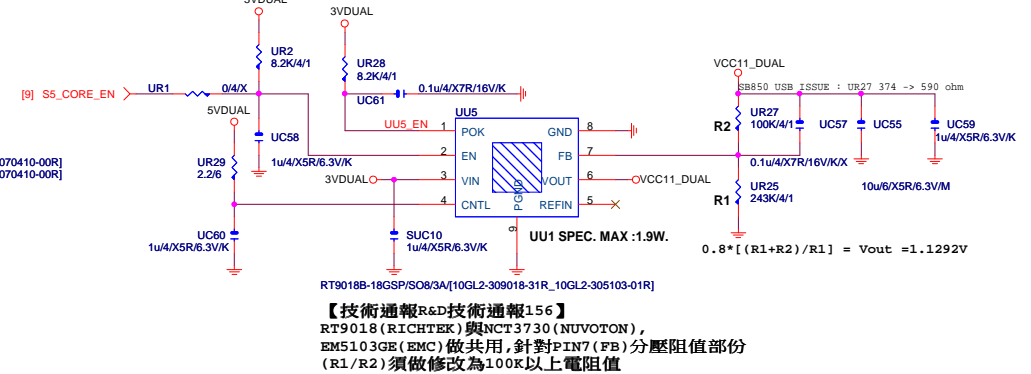
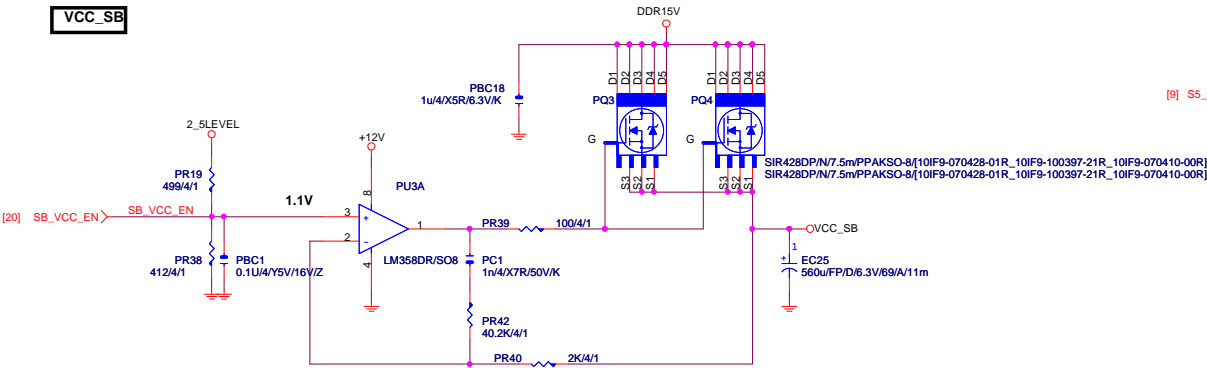






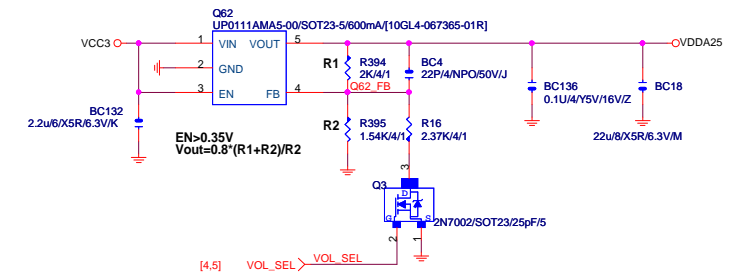
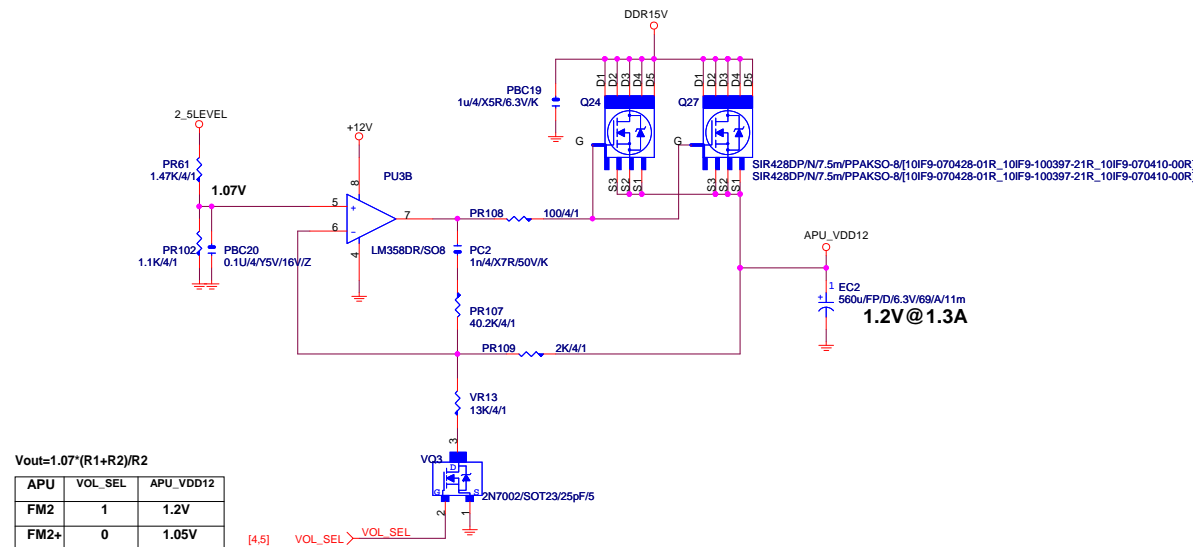


# VCC\_SB



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# APU\_VDDP



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

**GIGABYTE**

Title: **VCC\_SB, APU\_VDDP, VCC11\_DUAL, VDDA25**

Size: Custom

Document Number: **GA-F2A78M-HD2**

Rev: **3.0**

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